

120A, 100V N-CHANNEL MOSFET

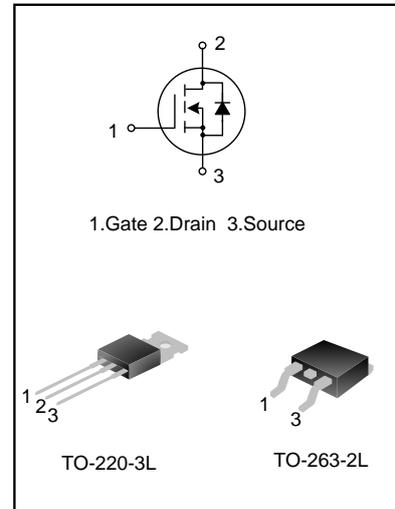
DESCRIPTION

SVG104R5NT(S) is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

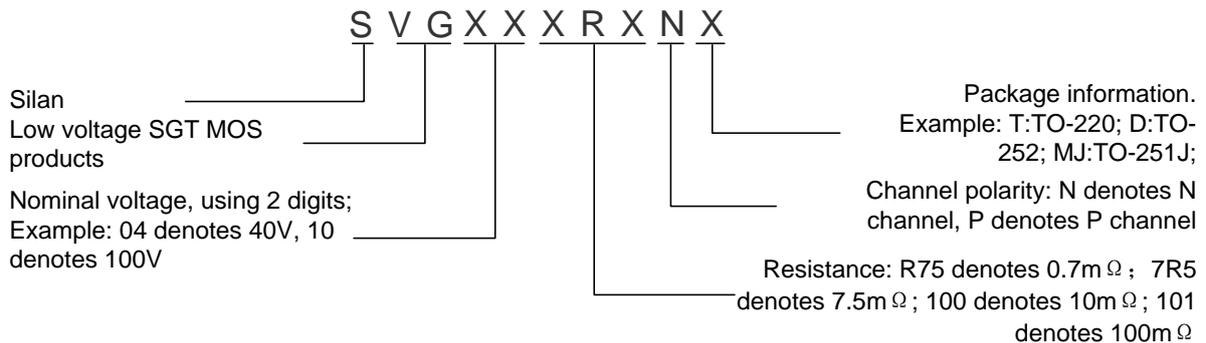
This device is widely used in UPS, Power Management for Inverter Systems.

FEATURES

- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability



NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVG104R5NT	TO-220-3L	104R5NT	Pb free	Tube
SVG104R5NS	TO-263-2L	104R5NS	Halogen free	Tube
SVG104R5NSTR	TO-263-2L	104R5NS	Halogen free	Tape&Reel

ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, $T_C=25^\circ\text{C}$)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	120	A
	$T_C=100^\circ\text{C}$		110	
Drain Current Pulsed		I_{DM}	480	A
Power Dissipation($T_C=25^\circ\text{C}$) -Derate above 25°C		P_D	208	W
			1.7	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy(Note 1)	$L=0.5\text{mH}$	E_{AS}	780	mJ
	$L=0.1\text{mH}$		450	mJ
Operation Junction Temperature Range		T_J	$-55 \sim +150$	$^\circ\text{C}$
Storage Temperature Range		T_{stg}	$-55 \sim +150$	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.6	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $T_C=25^\circ\text{C}$)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu\text{A}$	100	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=50A(\text{TO-220-3L})$	--	3.6	4.5	$\text{m}\Omega$
		$V_{GS}=10V, I_D=50A(\text{TO-263-2L})$	--	3.4	4.2	$\text{m}\Omega$
Gate Resistance	R_G	$f=1\text{MHz}$	--	2.4	--	Ω
Input Capacitance	C_{iss}	$f=1\text{MHz}, V_{GS}=0V, V_{DS}=50V$	--	7266	--	pF
Output Capacitance	C_{oss}		--	864	--	
Reverse Transfer Capacitance	C_{rss}		--	24	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, V_{GS}=10V, R_G=3\Omega, I_D=50A$ (Note 2,3)	--	32	--	ns
Turn-on Rise Time	t_r		--	50	--	
Turn-off Delay Time	$t_{d(off)}$		--	83	--	
Turn-off Fall Time	t_f		--	31	--	
Total Gate Charge	Q_g	$V_{DD}=50V, V_{GS}=10V, I_D=20A$ (Note 2,3)	--	114	--	nC
Gate-Source Charge	Q_{gs}		--	37	--	
Gate-Drain Charge	Q_{gd}		--	26	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction	--	--	120	A
Pulsed Source Current	I_{SM}	Diode in the MOSFET	--	--	480	
Diode Forward Voltage	V_{SD}	$I_S=50A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=50A, V_{GS}=0V,$	--	77	--	ns
Reverse Recovery Charge	Q_{rr}	$dI/dt=100A/\mu s$ (Note 2)	--	0.18	--	μC

Notes:

1. $V_{DD}=80V, R_G=25\Omega,$ starting $T_J=25^\circ C$;
2. Pulse Test: Pulse width $\leq 300\mu s,$ Duty cycle $\leq 2\%$;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. Output Characteristics

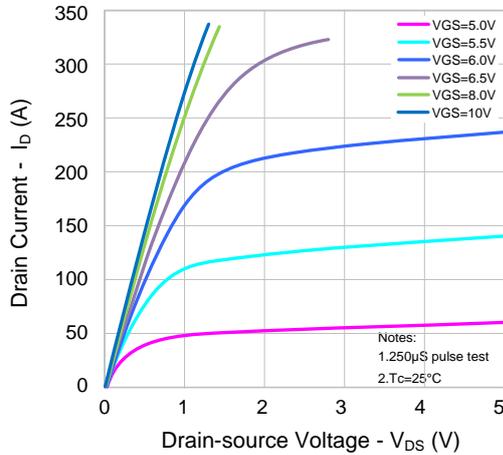


Figure 2. Transfer Characteristics

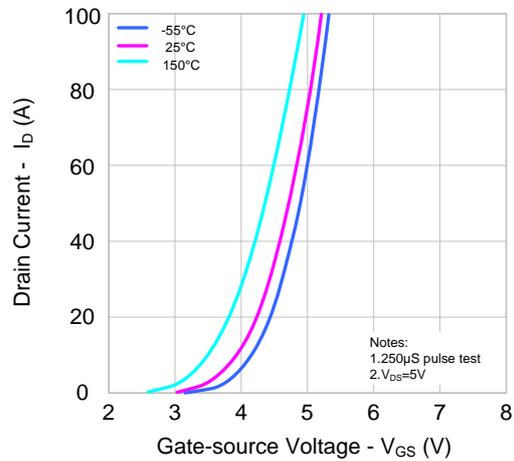


Figure 3. On-resistance vs. Drain Current

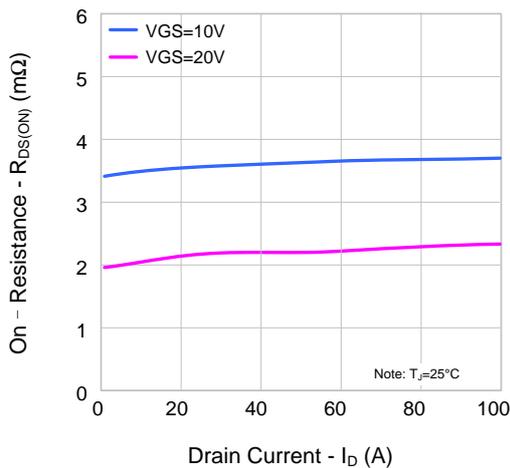


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

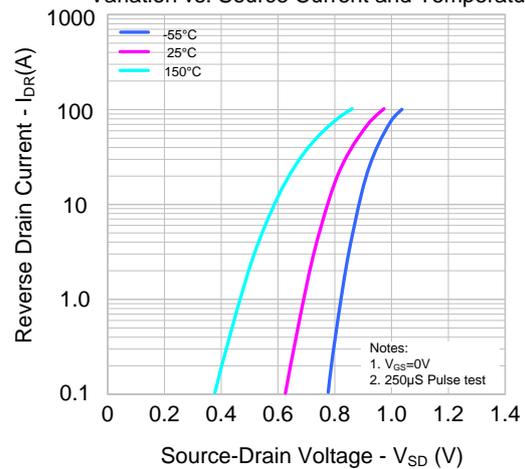


Figure 5. Capacitance Characteristics

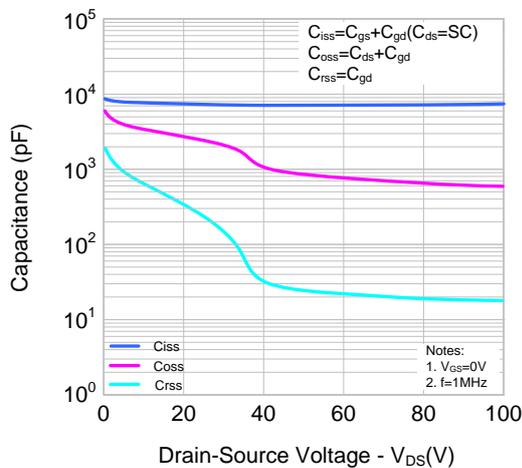
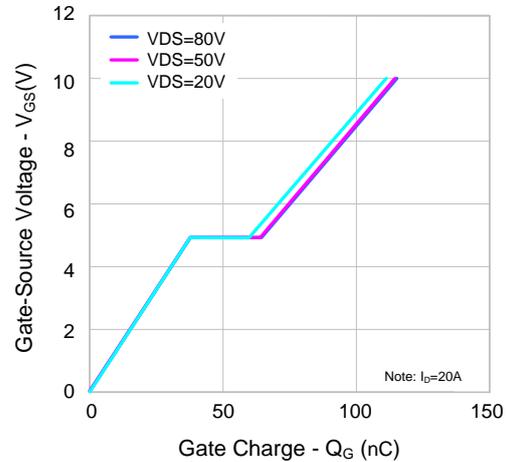


Figure 6. Gate Charge



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage vs. Temperature Characteristics

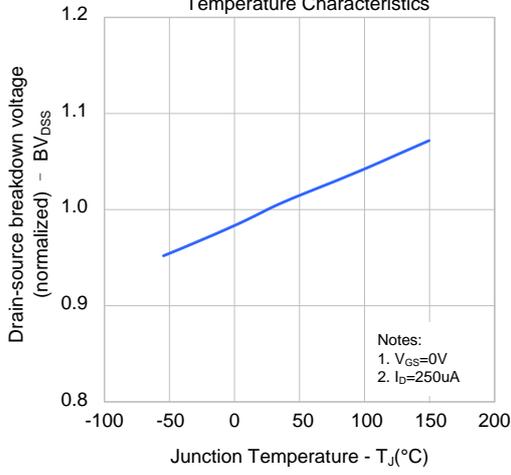


Figure 8. On-resistance vs. Temperature Characteristics

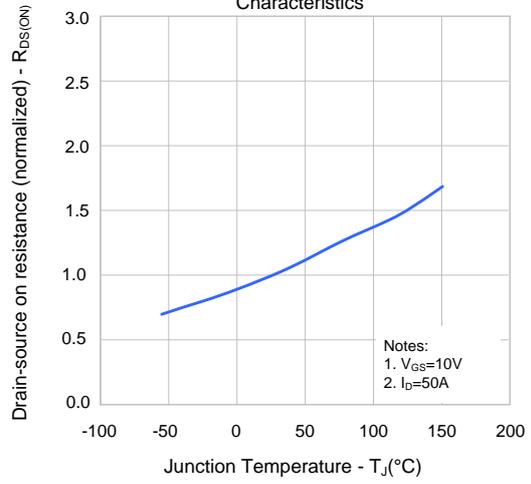
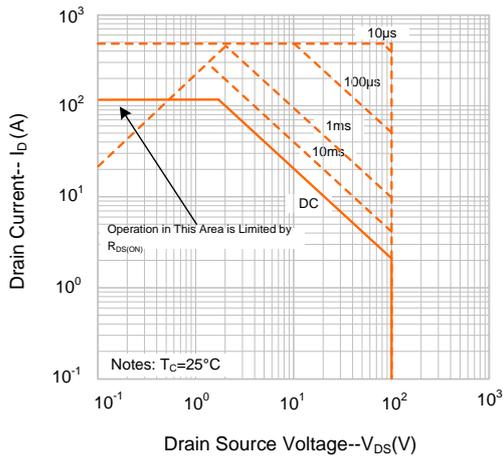
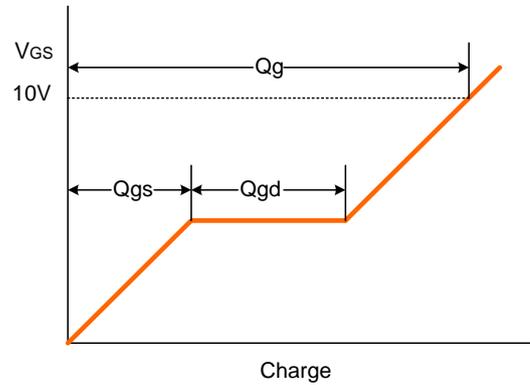
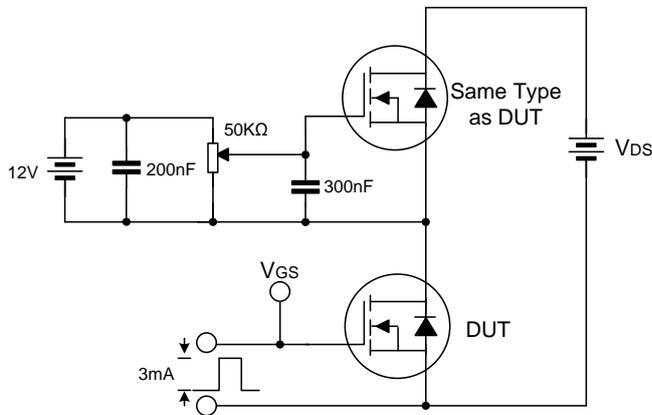


Figure 9. Max. Safe Operating Area

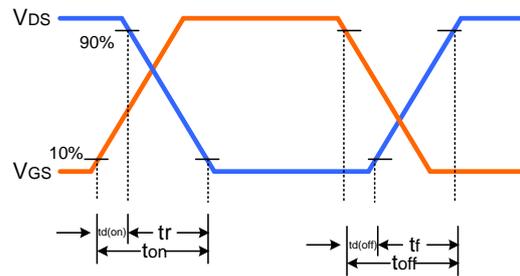
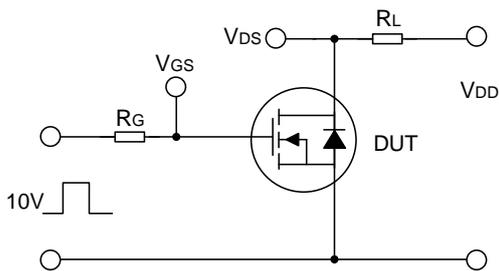


TYPICAL TEST CIRCUIT

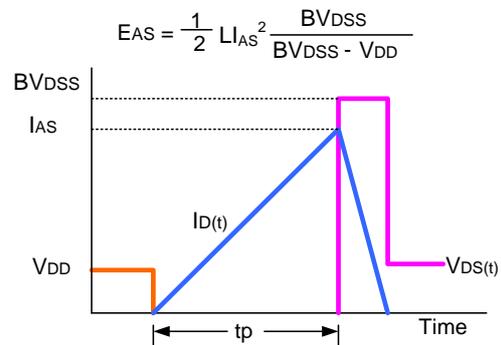
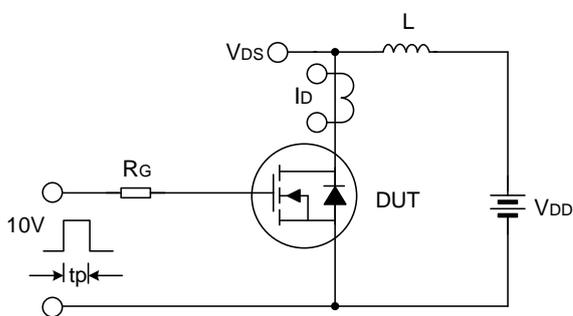
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



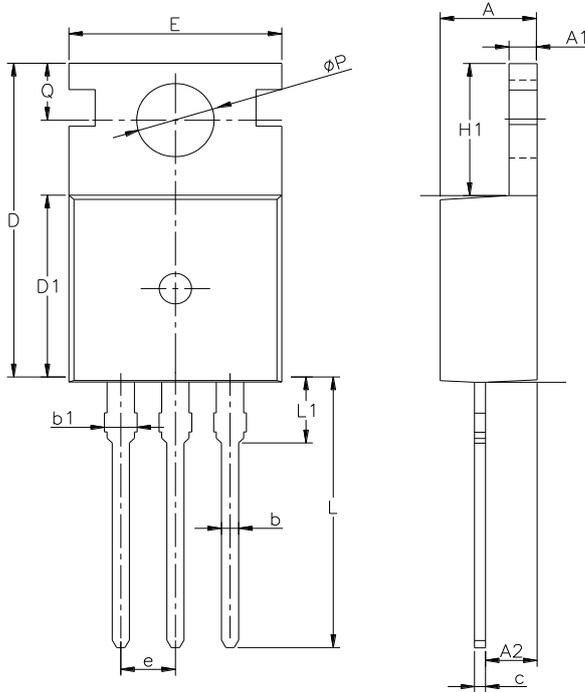
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220-3L

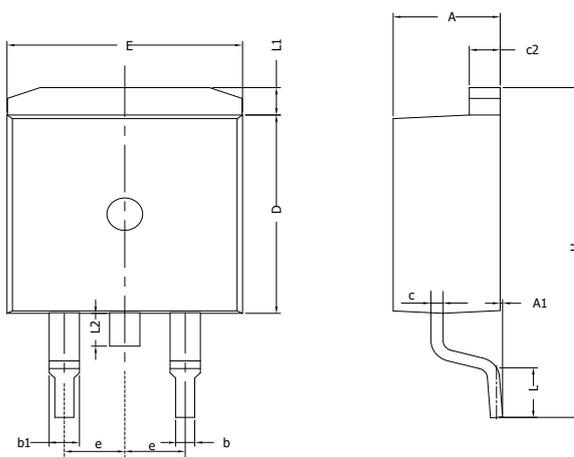
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ϕP	3.40	3.70	3.90
Q	2.60	—	3.20

TO-263-2L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
c	0.30	—	0.60
c2	1.17	1.27	1.37
D	8.50	—	9.35
E	9.80	—	10.45
e	2.54BSC		
H	14.70	—	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	—	—	1.75

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Rev.: 1.2

Revision History:

1. Add EAS value of L=0.1mH

Rev.: 1.1

Revision History:

1. Add TO-263-2L

Rev.: 1.0

Revision History:

1. First release
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